1. A method for the elimination of one or more redundant tests and the reordering of one or more inefficient tests in digital integrated circuits (IC's), further comprising:

for each test of a sequence of N tests, compiling L common defective dice, wherein said N tests comprise one or more redundant tests and one or more inefficient tests;

representing each test of the sequence of N tests as a correlation vector such that the sequence of N tests is represented as N correlation vectors;

finding a first correlation vector of the N correlation vectors that has the most non-zero components and initialize a vector W to be the complement of the first correlation vector;

for each correlation vector of the remaining N-1 correlation vectors, calculating a product of the complement of each correlation vector and the vector W;

calculating a length of a projection of each calculated product vector onto a unit vector;

finding the correlation vector of the N-1 correlation vectors that has a smallest value of the projection length;

updating the vector W to be a product of vector W and a compliment of the determined correlation vector in the previous

step; and

repeating the previous four elements, until the length of the projection of vector W onto the unit vector is zero.

2. The method of claim 1, wherein the correlation vector that has the smallest value of the projection length is stored as one of the correlation vectors in an optimized set.

3. The method of claim 1, wherein each correlation vector is represented using a binary-valued L-dimensional vector.

4. The method of claim 1, wherein a multiplication of two vectors is defined to be a vector which components are calculated from the logical AND operation of the corresponding components of the two vectors.

5. The method of claim 1, wherein the execution time of each test is the same.

6. The method of claim 1, wherein prior to compiling the N tests, executing the sequence of N tests without stopping at a failing test.

7. The method of claim 1, further comprising analyzing the correlation among the N tests by representing each test of the n tests in a L-dimensional defective die space using a binary-valued L-dimensional vector.

8. The method of claim 2, wherein finding a vector in the optimized set of vectors further comprises determining the vector of the remaining vectors with a smallest value of the square of the length of the projection of vector

W onto the unit vector.

9. The method of claim 1, wherein finding a vector of the optimized set further comprises all remaining vectors of the N correlation vectors with zero projection onto vector W representing zero defects.

10. The method of claim 1, further comprising obtaining the optimized set by sorting the lengths of the N projection vectors in a descending order.

11. A method for the reordering of one or more inefficient tests in digital integrated circuits (IC's) when the execution time of each test is the same, further comprising:

for each test of a sequence of N tests, compiling L common defective dice;

representing each test of the sequence of N tests as a correlation vector using a binary-valued L-dimensional vector;

finding a first correlation vector of the N correlation vectors that has the most non-zero components and initialize a vector W to be the complement of this first correlation vector;

defining a multiplication of two correlation vectors to be a vector with components calculated from the logical AND operation of the corresponding components of the two correlation vectors;

for each correlation vector of the remaining correlation vectors, calculating a product vector of the complement of each

correlation vector and vector W using the multiplication definition in the previous element;

calculating a projection length of each product vector onto the unit vector;

finding the correlation vector that has the smallest value of the projection length;

storing this correlation vector as one of the correlation vectors in an optimized sequence;

updating vector W to be the product of vector W and a compliment of the correlation vector in the previous step;

repeating the previous five elements, until the length of the projection of vector W onto the unit vector is zero; and

assigning the vector W to be the unit vector and repeating the previous six elements until there are no remaining vectors.

12. A method for the elimination of one or more redundant tests and the reordering of one or more inefficient tests in digital integrated circuits (IC's) when the execution time of each test is different, further comprising:

for each test of a sequence of N tests, compiling L common defective dice and storing the execution time of the sequence of N tests;

representing each test of the sequence N tests as a correlation vector using a binary-valued L-dimensional vector;

finding a first correlation vector of the N correlation vectors that has the largest value of the number of non-zero components divided by the execution time of the corresponding test and then initialize vector W to be a complement of this vector;

defining the multiplication of two correlation vectors to be a vector with components that are calculated from the logical AND operation of the corresponding components of the two correlation vectors;

for each correlation vector of the remaining correlation vectors, calculating a length of a projection of the correlation vector onto vector W;

calculating a quotient of the calculated projection length in the previous step and the execution time of the corresponding test;

finding the correlation vector that has the largest value of the quotient calculated in the previous step;

storing this correlation vector as one of the correlation vectors in an optimized sequence;

updating vector W to be the product of vector W and the compliment of the stored correlation vector in the previous step; and

repeating the previous five elements, until the length of the projection of vector W onto the unit vector is zero.

13. A method for the reordering of one or more inefficient tests in digital integrated circuits (IC's) when the execution time of each test is different, further comprising:

for each test of a sequence of N tests, compiling L common defective dice and storing the execution time of the sequence of N tests;

representing each test of the sequence of N tests as a correlation vector using a binary-valued L-dimensional vector;

finding a first correlation vector of the N correlation vectors that has the largest value of the number of non-zero components divided by the execution time of the corresponding test and then initialize a vector W to be a complement of this vector;

defining a multiplication of two correlation vectors to be a vector with components that are calculated from the logical AND operation of the corresponding components of the two correlation vectors;

for each correlation vector of the remaining correlation vectors, calculating a length of a projection of the correlation vector onto vector W;

calculating a quotient of the calculated projection length in the previous step and the execution time of the corresponding test;

finding a correlation vector that has the largest value of the quotient calculated in the previous step;

storing this correlation vector as one of the correlation vectors in an optimized sequence;

updating vector W to be the product of vector W and a compliment of the stored correlation vector in the previous step;

repeating the previous five elements, until the length of the projection of vector W onto a unit vector is zero; and

assigning vector W to be the unit vector and repeating the previous six elements until there are no remaining vectors.